Lunar Orbital Platform–Gateway Gigabit Ethernet Media Converter

Spring 2019 Engineering Capstone

By

Team 23

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Abstract

LOP–G is a planned space station that will orbit the moon. The variety of different communication standards aboard the station necessitates a converter to allow the different portions of LOP–G to interface with each other. Such a converter would have to obey strict timing requirements outlined by IEEE and SAE standards, as well as have radiation tolerance to be able to operate correctly in space. Team 23's goal was to design a prototype for such a converter and present it to Honeywell for further development. The prototype does not have the full functionality of a flight design, but Team 23 has also proposed a list of further steps to take to bring the prototype to flight–readiness. The prototype is able to convert bidirectionally between copper and fiber optic gigabit Ethernet signals, under a variety of power levels and electromagnetic interference. Results indicate that the prototype meets its specifications. The prototype correctly translates data bidirectionally between fiber optic and copper gigabit Ethernet signals. The data eye diagram is clean and fits within the eye mask defined by the IEEE gigabit Ethernet standard. The size, weight, and power parameters of the design are sufficiently minimized for the scope of the project. Future design steps include adding further EMI protection as well as improving temperature tolerance. These steps will allow the design to achieve full flight specification and ultimately be used aboard LOP–G as well as other future space missions. This capstone project was a success, and lays the groundwork for future innovation in electrical engineering.

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1 Introduction

The Lunar Orbital Platform–Gateway (LOP–G) is a planned collaborative space station headed by NASA and in conjunction with other major space agencies such as Roscosmos, ESA[1], and JAXA[2]. The goal is to send a space station to orbit the moon, where it will serve as a hub for scientific experiments, long–range communications, habitation, as well as a staging area for future space launches [1]. This opens up a variety of opportunities for cooperation between different nations as well as commercial partners to help further man's reach into the universe.

The complexity of LOP–G poses a problem for internal signaling and communications. In order to facilitate different modules properly interfacing with one another as well as with command centers located on Earth, it is necessary to use different networking technologies. For example, the different portions of the LOP–G will communicate through copper–based Ethernet networks, while communications with Earth will be through free–space optical terminals.

The use of multiple networking technologies necessitates a method to seamlessly convert between them. A simple media conversion solution allows the opportunity for facilitating this conversion while also reducing the Size, Weight, and Power (SWaP) footprint of the overall station. Given that the current cost of putting payloads into Earth orbit lies in the ballpark of $10,000 USD per kilogram [2], it becomes readily apparent why reducing the SWaP footprint is important.

Another important consideration is the use of Commercial Off–The–Shelf (COTS) components. Such components are both readily available, reducing their cost, and proven in the field, increasing their reliability. Thus, incorporating COTS components into the design of a media converter has significant benefits for the LOP–G program as a whole.

The goal of this capstone project, titled "Lunar Orbital Platform–Gateway Ethernet Media Converter", was to create a prototype for such a converter. The project was sponsored by Honeywell Aerospace, a major aerospace company with an interest in designing and ultimately providing the final flight–ready media converters for the station.

[1] European Space Agency
[2] Japanese Aerospace Exploration Agency

2 Approach

2.1 Specifications

To keep the scope of the project realistic, the proposed media converter design only converts between two of the many different Gigabit Ethernet (GbE) standards. The two selected were:

- 1000BASE–CX copper GbE
- 1000BASE–SX fiber optic GbE

These standards were chosen due to the fact that both are common in commercial usage, so their respective COTS components are relatively easy to find.

The media converter prototype had the following design requirements, based on the research conducted and feedback from the team's mentors:

- Convert bidirectionally between each GbE standard
- Operate using a 28 V supply rail[1][3]
- Generate minimal levels of Electromagnetic Interference (EMI)
- Tolerate EMI at levels common for space vehicle environments[2]
- Tolerate power supply voltage spikes from lightning striking the launch vehicle during launch and ascent

In addition, the design had the following goals:

- Minimize SWaP footprint
- Use mostly COTS components

The engineering standards which the prototype design should adhere to are IEEE[3] 802.3, which covers basic Ethernet requirements such as timing (see Tables 1–4) [4], and SAE[4] AS6802, which covers the "fault–tolerant synchronization strategy" used in automotive applications [5].

[1]Common in many space vehicle electrical systems
[2]In this case, the radiation environment was assumed to be similar to Low–Earth Orbit (LEO)
[3]Institute of Electrical and Electronics Engineers
[4]SAE International

Description	Value	Unit
Type	(P)ECL	
Data rate	1000	Mb/s
Clock tolerance	±100	ppm
Nominal signaling speed	1250	MBd
Differential amplitude (p-p)		
Max (worst case p-p)	2000	mV
Min (opening)	1100	mV
Max (OFF)[a]	170	mV
Rise/Fall time (20-80%)		
maximum	327	ps
minimum	85	ps
Differential skew (max)	25	ps

[a]Examples of an OFF transmitter are no power supplied to the PMD and PMA transmit output being driven to a static state during loopback.

Table 1: Transmitter characteristics for 1000BASE–CX (copper) gigabit Ethernet, taken from IEEE 802.3 Table 39–2, "Transmitter characteristics at TP2" [4].

Description	Value	Units
Data rate	1000	Mb/s
Nominal signaling speed	1250	MBd
Tolerance	±100	ppm
Minimum differential sensitivity (peak-peak)	400	mV
Maximum differential input (peak-peak)	2000	mV
Input Impedance @ TP3		
TDR Rise Time	85	ps
Exception_window[a]	700	ps
Through_connection	150 ± 30	Ω
At Termination[b]	150 ± 10	Ω
Differential Skew	175	ps

[a]Within the Exception_window no single impedance excursion shall exceed the Through_Connection-impedance tolerance for a period of twice the TDR rise time specification.

[b]The input impedance at TP3, for the termination, shall be recorded 4.0 ns following the reference location determined by an open connector between TP3 and TP4.

Table 2: Receiver characteristics for 1000BASE–CX (copper) gigabit Ethernet, taken from IEEE 802.3 Table 39–4, "Receiver characteristics (TP3)" [4].

Description	62.5 µm MMF	50 µm MMF	Unit
Transmitter type	Shortwave Laser		
Signaling speed (range)	1.25 ± 100 ppm		GBd
Wavelength (λ, range)	770 to 860		nm
T_{rise}/T_{fall} (max; 20%-80%; λ > 830 nm)	0.26		ns
T_{rise}/T_{fall} (max; 20%-80%; λ ≤ 830 nm)	0.21		ns
RMS spectral width (max)	0.85		nm
Average launch power (max)	See footnote [a]		dBm
Average launch power (min)	–9.5		dBm
Average launch power of OFF transmitter (max)[b]	–30		dBm
Extinction ratio (min)	9		dB
RIN (max)	–117		dB/Hz
Coupled Power Ratio (CPR) (min)[c]	9 < CPR		dB

[a]The 1000BASE-SX launch power shall be the lesser of the class 1 safety limit as defined by 38.7.2 or the average receive power (max) defined by Table 38–4.
[b]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a "transmit disable" or other optional module laser shut down conditions. During all conditions when the PMA is powered, the ac signal (data) into the transmit port will be valid encoded 8B/10B patterns (this is a requirement of the PCS layers) except for short durations during system power-on-reset or diagnostics when the PMA is placed in a loopback mode.
[c]Radial overfilled launches as described in 38A.2, while they may meet CPR ranges, should be avoided.

Table 3: Transmitter characteristics for 1000BASE–SX (fiber optic) gigabit Ethernet, taken from IEEE 802.3 Table 38–3, "1000BASE–SX transmit characteristics" [4].

Description	62.5 µm MMF	50 µm MMF	Unit
Signaling Speed (range)	1.25 ± 100 ppm		GBd
Wavelength (range)	770 to 860		nm
Average receive power (max)	0		dBm
Receive sensitivity	–17		dBm
Return loss (min)	12		dB
Stressed receive sensitivity[a, b]	–12.5	–13.5	dBm
Vertical eye-closure penalty[c]	2.60	2.20	dB
Receive electrical 3 dB upper cutoff frequency (max)	1500		MHz

[a]Measured with conformance test signal at TP3 (see 38.6.11) for BER = 10^{-12} at the eye center.
[b]Measured with a transmit signal having a 9 dB extinction ratio. If another extinction ratio is used, the stressed receive sensitivity should be corrected for the extinction ratio penalty.
[c]Vertical eye-closure penalty is a test condition for measuring stressed receive sensitivity. It is not a required characteristic of the receiver.

Table 4: Receiver characteristics for 1000BASE–SX (fiber optic) gigabit Ethernet, taken from IEEE 802.3 Table 38–4, "1000BASE–SX receive characteristics" [4].

2.2 Management

In order to create a prototype design, the team created a development flow, summarized in Fig. 1. The work was split into four major phases. During phase one, the team researched to determine the design specifications. During phase two, the team selected the components for the design. Phase three consisted of iterating a PCB design with feedback from the team's mentors. During phase four, testing was conducted at Honeywell facilities to ensure the prototype matched its specifications.

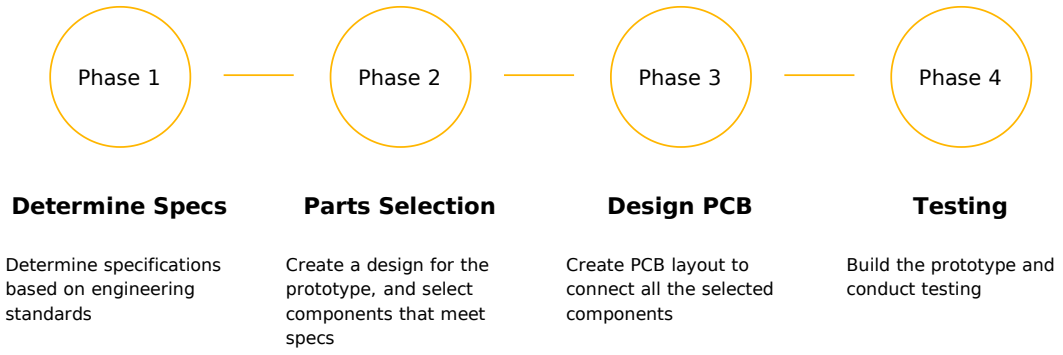


Figure 1: The workflow used to create and build the converter prototype.

The timeline followed to implement this flow is shown in Table 5:

Date	Task
9/06/18	Team formed
11/28/18	Research completed
1/05/18	Components selected
2/24/18	Initial circuit designed
4/05/19	PCB layout completed
4/12/19	Prototype built
4/20/19	Testing
4/26/19	Presentation

Table 5: The final schedule for the development of the converter prototype.

The design had a total budget of $1100. $100 of this was provided by Arizona State University (ASU), while the remaining $1000 was provided by Honeywell. The total costs incurred were $433.33. The cost of the prototype is $481.66. Cost breakdowns are shown in Tables 8–9 (see Appendix B).

The total cost is approximately double that of the prototype sans quadrax adapter (which

was provided for free by Honeywell) because for safety and redundancy, the team decided to build two identical copies of the design. This was inspired by the mentors' lab methodology, in which each hardware component had multiple identical backup components for redundancy.

Additionally, each team member spent approximately 4 hours each week between team formation and designing the initial circuit (24 weeks), and 6 hours each week until testing was completed (8 weeks). The final week, each team member spent 14 hours working on the project. This sums to 632 man–hours spent researching, developing, building, and testing the prototype, as well as writing reports.

2.3 Work Conducted

The first step to meeting the converter specifications was to conduct research. The team obtained copies of the IEEE and SAE standards and thoroughly reviewed the relevant sections regarding 1000BASE–SX and 1000BASE–CX transmitter and receiver characteristics. These sections specify signal rise and fall times, amplitudes, the range of acceptable optical wavelengths for lasers and photoreceivers, and more. All of these specifications are contained within clauses 38 and 39 of the IEEE standard [4], respectively. Once the team gained an idea of the specific requirements outlined in the standards, the next step was to select suitable components.

The team split into two groups of two, focusing on fiber optic transceivers and copper transceivers, respectively. Each team created a list of components that matched the specifications, before reconvening to select the ones which were ultimately used. The team as a whole also selected other relevant components, such as the connector ports and power converter.

Once the components were selected, a preliminary block diagram describing how the signal I/O on the transceivers would be connected to each other. This block diagram was used to create a circuit, which was then iterated several times to improve the design. Once the circuit was finalized, a PCB was drafted using Altium Designer® 18. The PCB design was iterated several times, incorporating feedback from the mentor to improve the design.

Once the PCB design was finalized, it was sent to Advanced Circuits, a PCB manufacturer. The other components were ordered from Digi–Key Electronics. When the components and PCB arrived, the team used solder paste to attach the components to the board. The finished prototype was then taken to Honeywell for testing using the specialized equipment located there.

2.4 Component Selection Methodology

Components were evaluated against a number of criteria before being selected. Most importantly, components were selected based on their applicability in the design. During phase 1 (see Fig. 1), the team compiled a list of parts that had the correct characteristics to be used in the prototype. After the initial list was formed, the team compared the parts based on several criteria.

The availability of each part was an important consideration. A few of the components initially

considered were no longer being produced. For example, the PulseR copper transceiver Integrated Circuit (IC) was no longer in production when the project began. Luckily, the team was able to contact PulseR's sales team, which sent Team 23 three samples of the PulseR IC and an evaluation kit. If the team had not been able to obtain these samples, a different transceiver chip would have been needed.

Cost was another factor in Team 23's part selection. Price played a determining role when the team completed a draft of the 4–layer circuit board and wanted to use a custom layer stackup, where the layers of dielectric material were set to very specific thicknesses to help obtain the correct differential pair impedances. However, Advanced Circuits advised the team that this would not be possible within the desired price range. Therefore, it became necessary to use a standard layer stackup and to redesign as necessary.

Manufacturability was also a consideration in the design process. The team originally intended to use a Maxim Integrated Circuits MAX3711 transceiver and limiting amplifier in conjunction with discrete Transmitter Optical Sub–Assembly (TOSA) and Receiver Optical Sub–Assembly (ROSA) components for the fiber optic portion of the design. This would have given the team design control over the LED and photoreceiver characteristics for the optical transmitter and receiver. This approach would have also been more cost–effective than using a Small Form–factor Pluggable (SFP) module. However, the MAX3711 presented two major problems:

1. It was so small that soldering it to the PCB was not possible with the available equipment. Additionally, one of the mentors advised that it would be impossible to use this part without specialized automated soldering equipment.
2. It required a microcontroller to reprogram it at every start–up.

To avoid manufacturability problems and over–complicating the design, the team decided to use a small SFP module from Avago Technologies instead.

The team strove to keep the design as simple and robust as possible in other fields as well. Due to the power requirements of the transceiver modules, the design needed to convert an externally applied 28 V to 3.3 V. After conducting initial research, the team learned it was possible to design a custom DC/DC converter using several small circuit elements—a buck converter, a diode array, and various RLC[1] components. Furthermore, a custom DC/DC converter can provide a higher efficiency. A custom power supply design offers fine–tuning control over operational temperature range, nominal input voltage, input voltage range, and current output. However, the additional complexity introduces additional potential points–of–failure, which ultimately led the team to opt for a discrete DC/DC converter module solution instead, the TRACO TMR2410.

2.5 Design

The design uses the following components:

[1]Resistors, capacitors, and inductors

- PulseR Ruggedized Solutions TM1250HSB5 Integrated Circuit (IC) copper GbE transceiver
- Avago Technologies HFBR–5911LZ Small Form–factor Pluggable (SFP) fiber optic GbE transceiver
- TRACO Power TMR 2410 DC–DC converter
- Amphenol Aerospace 150 Ω PCB Quadrax Receptacle 90° Adapter/Tail Length 0.110
- Resistors, Surface Mount (SMD) 1206 size (various)
- Capacitors, SMD 1206 size (various)
- LEDs, SMD 1206 size (various)

The fiber optic and copper transceivers pose an issue in that they operate in different logic families: the fiber optic transceiver uses Low–Voltage Positive Emitter–Coupled Logic (LVPECL), while the copper transceiver operates on Current Mode Logic (CML). The specifications for both transceivers can be found in Table 6. Since the fiber optic transceiver has a higher output voltage swing than the input of the copper transceiver, the design must have a logic conversion to be able to send signals from one transceiver to the other.

Transceiver	**Operating Temperature**	**Voltage Swing** ($\mathrm{mV_{pp}}$)	
		Input	Output
TM1250HSB5	−55 °C to 125 °C	600	500
HFBR–5911LZ	−10 °C to 85 °C	1200	900

Table 6: Characteristics of the transceiver components used in the prototype [6],[7].

The circuit diagram for the logic translation can be seen in Fig. 2. In this diagram, it is possible to see how this conversion between logic families is accomplished. Each transceiver receives data and sends it out of the RD port to the other transceiver's TD ports to transmit. The DC bias of each differential signal is removed internally by each transceiver, so the main task is to attenuate the fiber optic to copper signal path. The path from the RD of the fiber optic transceiver has a Π–pad attenuator on each signal trace, to reduce the differential signal voltage from 900 $\mathrm{mV_{pp}}$ to 600 $\mathrm{mV_{pp}}$. The copper to fiber optic signal path does not need to be attenuated. The signal traces each have a pull–down resistor to eliminate charge build–up.

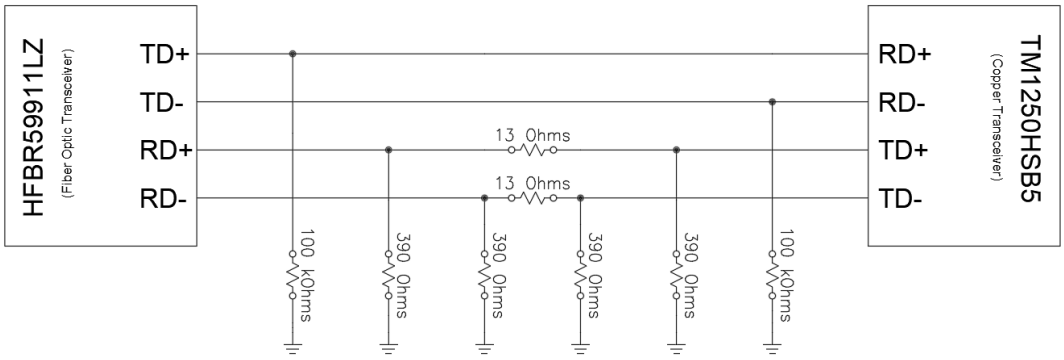


Figure 2: The circuit diagram representing the inter–transceiver logic translation scheme.

Note that the component selection leads to further design simplification. Because both the chosen transceivers contain internal coupling capacitors, the signal traces do not need to be AC coupled and are instead DC–balanced, which isolates the signal from external noise on the power rail which can be transmitted through the DC–biasing circuitry.

The chosen components also give the design some measure of inherent Electrostatic Discharge (ESD) and EMI protection. The copper GbE transceiver is internally transformer–coupled with a dielectric rating of 1500 V [6]. On the 1000BASE–SX side, optical fiber is naturally non–conductive and ESD–immune [8].

The design circuit schematic implementing the signal and power conversion is shown in Fig. 11–12 (see Appendix A). The PCB design is shown below in Fig. 3–4. These implement the design, and add probe points and LEDs used to check if the design is functioning correctly. The addition of a chassis ground is used to further protect the design against ESD, to allow direct conductive bonding to the enclosure.

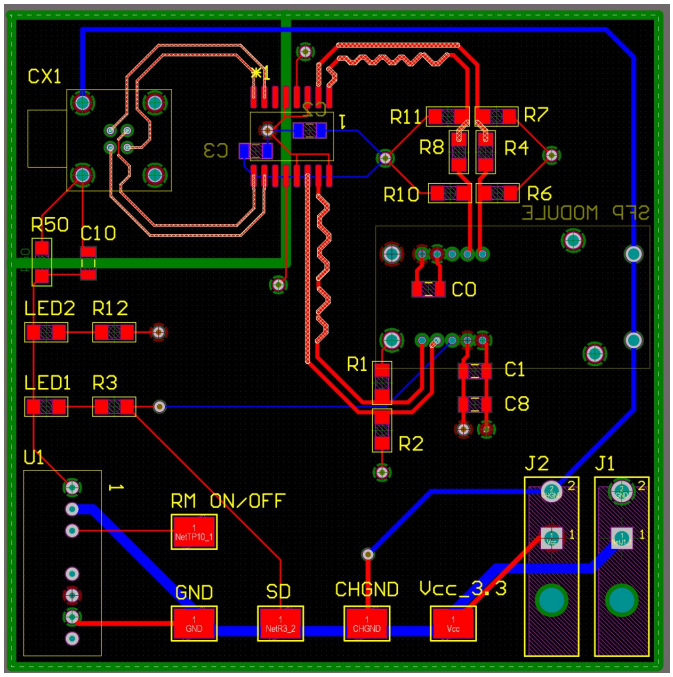
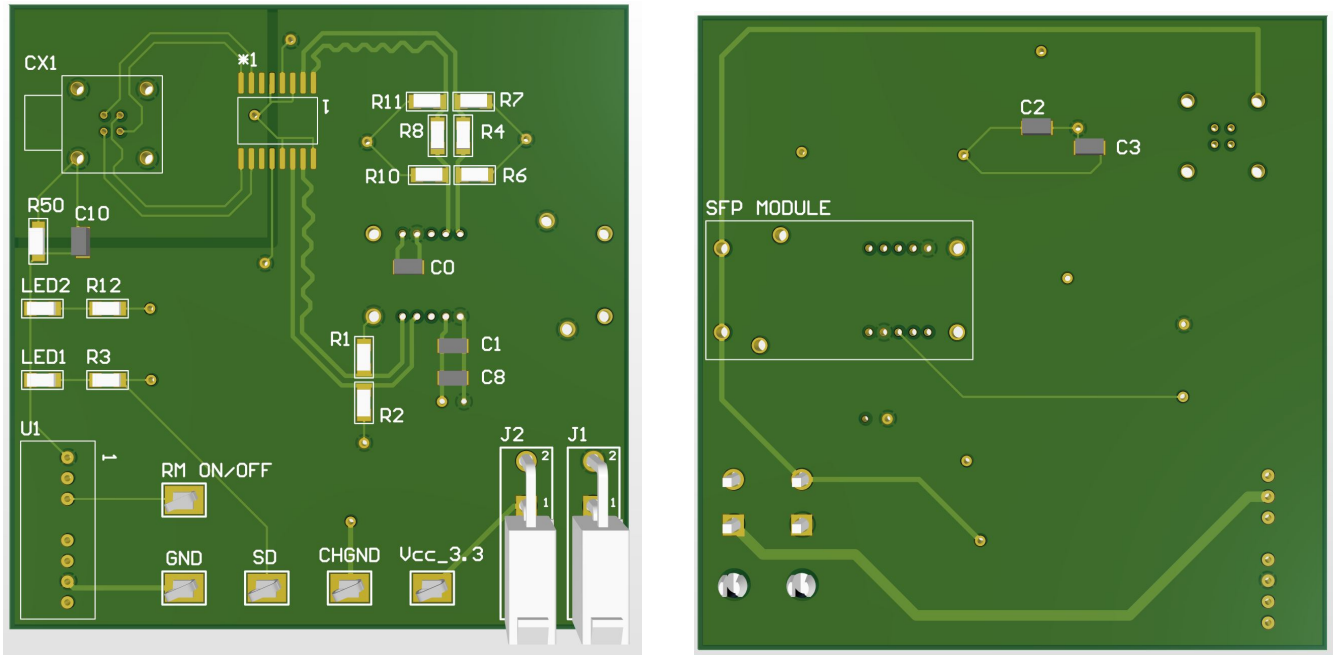


Figure 3: The PCB layout of the design.



(a) Front (b) Back

Figure 4: 3–dimensional simulated views of the front and back of the PCB.

The completed and built design is shown below in Fig. 5.

(a) Front

(b) Back

Figure 5: The completed prototype.

It should also be noted that each of the integrated circuits on the design are connected to power with decoupling capacitors nearby. Using decoupling capacitors on the V_{CC} lines fulfills several functions. First, they act as a low–pass filter, to reduce inrush current that could damage the ICs. Additionally, as the ICs switch states during operation, their current draw rapidly fluctuates. Placing capacitors near their V_{CC} inputs provides a small reserve from which the ICs can draw without placing high frequency demands on the DC/DC converter.

Team 23 faced a challenge when impedance matching the data transmission lines on the PCB. Both the LVPECL and CML logic families use differential signaling, so each signal requires two traces that are matched in length, properly spaced, and adequately distanced from the board's internal ground plane to ensure the signals arrive uncorrupted.

The prototype operates at around 1 Gbps. At such high frequencies, it is important to match the length of the differential lines as closely as possible. For example, pulse rise and fall times need to be about 0.1 ns in duration [4]. Generally, electrical pulses travel through copper at just over $0.5\,\frac{\text{ft}}{\text{ns}}$. According to the mentors, this means that lengths of differential pairs of transmission lines should be matched to within 0.050 in (50 mil). In the final design (see Fig. 3), all differential pairs of traces are length–matched to within 28 mil.

Additionally, differential–pair transmission lines need to be impedance matched with each other and with the ground plane. The application notes for both the PulseR transceiver chip and the Avago SFP module recommended that data transmission lines be matched at 100 Ω differential, and 50 Ω to ground to prevent signal reflection and "ringing" [6],[7]. On the copper side, the transmission lines connecting the transceiver to the quadrax connector were recommended to be set at 150 Ω differential impedance [6]. The design parameters that can be manipulated to control the impedance of each differential pair are:

- Thickness of dielectric between ground plane and transmission lines

- Relative permittivity ϵ of the dielectric
- Thickness of transmission line traces
- Spacing of transmission line traces
- Width of transmission line traces

The design uses a 4–layer PCB which uses the dielectric material FR–4, with a 10 mil thick layer between the top layer (signal layer) and first internal plane (ground plane). These values were chosen because they brought the PCB within our price range. The thickness of the transmission lines was set to 1.35 mil, the standard thickness for a 1 $\frac{\text{oz Cu}}{\text{in}^2}$[1] board [9]. The spacing of the transmission lines was set to 50 mil separation because the PulseR chips pins were spaced 50 mil apart (center–to–center). The width of the traces was varied as needed to get the desired impedance. For the 100 Ω matched lines, the traces were set to 10 mil in width. For the 150 Ω matched lines, the traces were set to 21 mil in width. All impedance calculations were checked with tools such as an impedance calculator[2].

2.6 Testing

The testing methodology for the prototype was developed based on the IEEE and SAE standards and the design specifications:

1. The prototype should be able to maintain a steady on–board supply voltage of 3.3 V when the LOP–G supply rail has a nominal voltage of 28 V and a maximum variance of 4 V. This is tested by varying the off–board supply input from 24 V to 32 V and observing the prototype's on–board supply voltage. The passing outcome is for the on–board supply to stay at 3.3 V.
2. The prototype should be able to convert signals bidirectionally during normal operation conditions. This is tested in two phases:
   (a) The off–board supply input is held steady at 28 V. Two computers ping each other through the converter ("TX") using fiber optic and copper wire signals simultaneously, and the converted fiber optic and copper wire signals are read on the other side ("RX"). Each computer then passes back a reply ping. The passing outcome is for the computers to both receive a reply to the pings.
   (b) The same test is repeated but the off–board supply input is varied from 24 V to 32 V. The passing outcome is for each computer to receive a reply to the pings.
3. The prototype should not convert signals when powered off. This is tested by removing the off–board supply input and then continuing to ping. The passing outcome is for each computer to not receive a reply, so the ping request will time out.

[1] Cu refers to copper
[2] `www.eeweb.com/tools/edge-coupled-microstrip-impedance`

4. The prototype should meet timing requirements defined in IEEE 802.3. This is tested by sending a fiber optic TX signal, and using a specialized oscilloscope to create an "eye diagram" of the copper wire RX signal. The passing outcome is for the eye diagram to fit within the constraints of the eye mask defined in IEEE 802.3 (see Fig. 6 below).

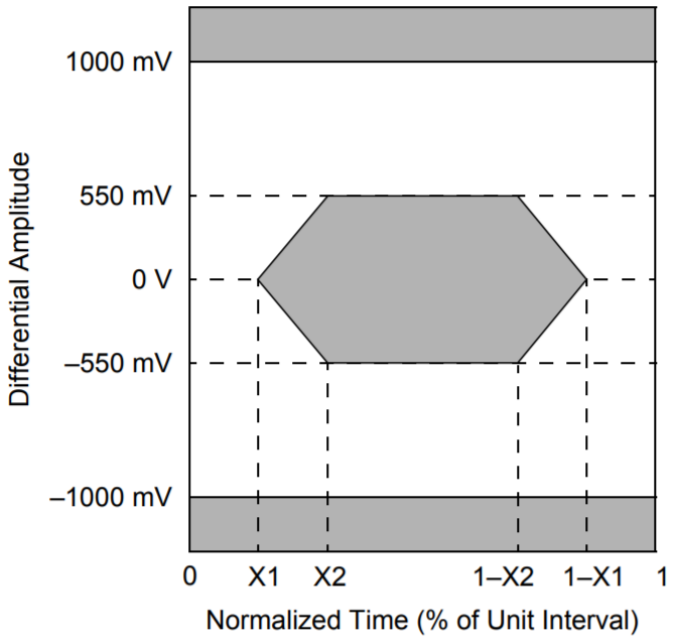
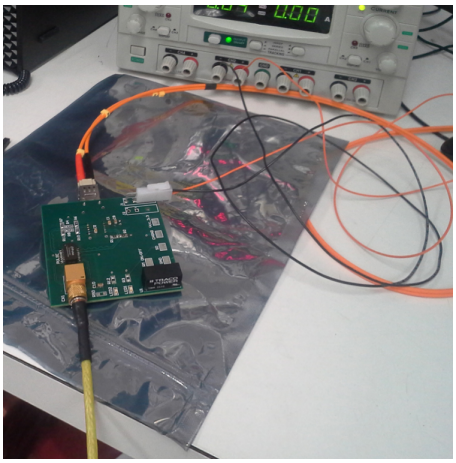


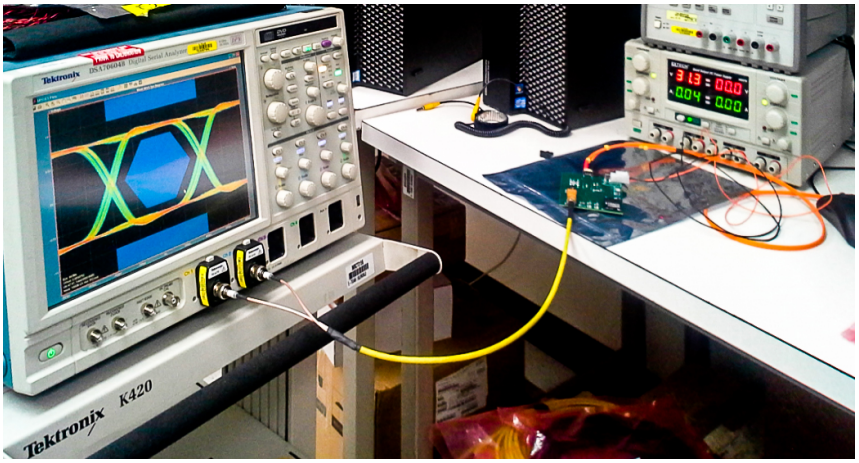
Figure 6: The data eye mask requirements provided in IEEE 802.3 Fig. 39–4, "Absolute eye diagram mask at TP2" [4]. The values given in the standard for X1 and X2 are 0.14 and 0.34, respectively.

5. The prototype should be able to survive large levels of input surge voltage (over–voltage), such as from lightning. This is tested by setting the off–board supply input to 40 V, then back to 28 V and repeating Test 2. The passing outcome is for the pings and replies to continue once the off–board supply input is reduced. Due to the fact that failing this test will permanently destroy the prototype, this test must be conducted last.

The testing setup can be seen in Fig. 7.



(a) PCB Connections



(b) Full Testing Setup

Figure 7: The PCB connections used in the testing setup.

3 Results

1. The prototype was able to maintain a steady on–board supply voltage of 3.296 V when the external supply was varied from 24 V to 32 V (see Fig. 13, Appendix A).
2. The prototype was able to convert signals bidirectionally (see Fig. 8a):
   (a) Both computers continuously received replies to the pings.
   (b) Each computer continuously received replies to the pings.

```
C:\Users\andysey\Documents>ping -t 10.2.2.15

Pinging 10.2.2.15 with 32 bytes of data:

Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
```

(a) On

```
C:\Users\andysey\Documents>ping -t 10.2.2.15

Pinging 10.2.2.15 with 32 bytes of data:

Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Reply from 10.2.2.15: bytes=32 time<1ms TTL=64
Request timed out.
Request timed out.
Request timed out.
Request timed out.
```

(b) Off

Figure 8: The result of two computers pinging each other via the converter, while the prototype is powered on and then turned off.

In addition, the data eye has the correct period, 800 ps, to correspond with the data transmission frequency, 1.25 GHz (see Fig. 9).

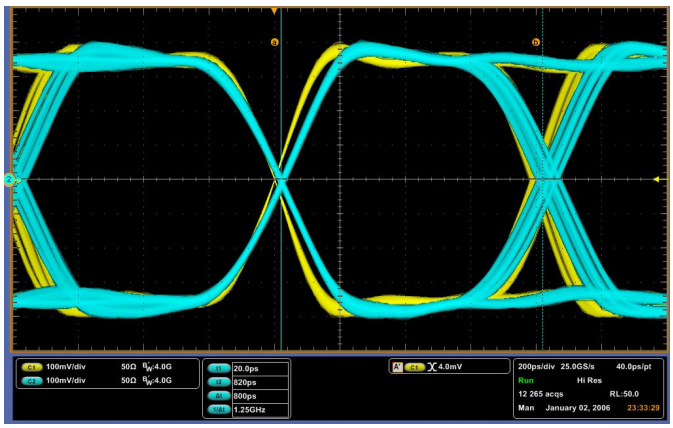
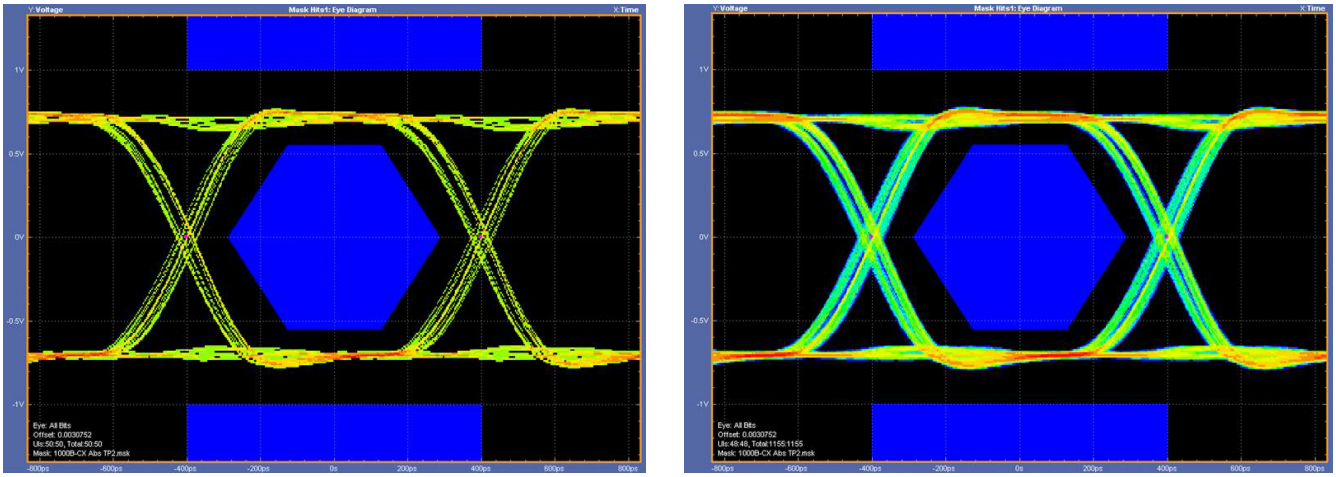


Figure 9: The data eye waveform for each differential line in the signal.

3. The prototype did not convert signals when powered off. Neither computer received a reply, and the ping requests timed out (see Fig. 8b).
4. The prototype met the timing requirements. The eye diagram fits within the constraints of the eye mask defined in IEEE 802.3 (see Fig. 10).



(a) Single (b) Continuous

Figure 10: The data eye diagram set against the eye mask requirements from IEEE 802.3, seen in Fig. 6, using single and continuous data capture.

5. The prototype was able to survive the off–board supply input to 40 V. The computers continued to successfully ping each other as anticipated once the voltage was lowered.

In addition, the static power dissipation was 952 mW at $V_{ext.} = 28$ V (see Table. 7). The prototype weighed 48 g and had a size of 7.8 cm × 9.9 cm.

External Voltage	**Area**	**Weight**	**Power**
24 V	7.8 cm × 9.9 cm	48 g	936 mW
28 V			952 mW
32 V			928 mW

Table 7: The SWaP parameters of the design. Power was calculated based off the results in Fig. 13.

4 Discussion

4.1 Data Analysis

The results gave the following conclusions regarding each test:

1. The steady voltage output indicates that the power converter is functioning as desired. Thus, this test was passed.
2. The continuous ping replies on both computers indicate that the converter was continually, bidirectionally translating the signal between copper and fiber optic GbE. Therefore, this test was passed.
3. The continuous ping request time out indicates that the converter does not function when there is no power provided, as expected. Therefore, this test was passed.
4. The eye diagram has a clean characteristic with well–defined borders. The data eye is also not close to touching the eye mask, which indicates that there will not be any faulty data. Therefore, this test was passed.
5. The prototype's continued operation after the voltage spike indicates that the device is protected from over–voltage to the desired degree. Therefore, this test was passed.

The SWaP parameters (given in Table 7) also show that the design occupies a relatively small area, is very lightweight, and minimizes power consumption.

4.2 Project Requirements

The converter design passed each test, indicating that it fulfills both the project specifications and the IEEE and SAE standards. Thus, the media converter prototype design was successful. It is able to survive large voltage spikes, operate under varying power levels, and bidirectionally convert data between fiber optic and copper GbE signals.

4.3 Future Design Improvements

The following design improvements should be implemented to create a final flight–ready design.

1. Add additional transceivers and conversion logic to implement the other Ethernet standards used on LOP–G.
2. Add the following circuits to the front–end of the power converter to further protect the design from EMI and long–term damage:

(a) EMI filter, which mitigates high–frequency noise in the supply rail.

(b) Inrush current limiter, which reduces the instantaneous surge current when turning on the device.

(c) Transient voltage suppressor, which protects against extremely fast voltage spikes.

3. Add an enclosure with a metal (aluminum or similar light–weight material) layer to act as a Faraday cage, further shielding the converter from EMI.

4. Increase the operational temperature range. The desired temperature range in military grade, or $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$ [10]. While the copper transceiver, TM1250HSB5, has an operational temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$ [6], the fiber optic transceiver, HFBR–5911LZ, only has an operational temperature range of $-10\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$ [7], which is less than the desired range. Thus, a flight design must substitute the fiber optic component for one with greater temperature tolerance.

5. The prototype had an issue that seemed to be caused by the size of the through–hole VIAs[1] short–circuiting the ground and power planes of the PCB. This issue can be amended by specifying that the cut–out holes in the ground and power planes be larger.

6. Replace the components chosen with more custom designs that utilize smaller COTS components to give greater design control, such as splitting the fiber optic transceiver into a signal translator (e.g. MAX3711) and TOSA/ROSA components

[1] Vertical interconnect access

5 Conclusion

In September 2018, Team 23 formed with the goal of designing a fiber to copper bidirectional Ethernet media converter for space applications. This project definition was very broad, and much of the first semester was spent narrowing down exactly what the final prototype should do. Considerable time was spent reducing the project scope to be both more achievable given the time, budget, and resource limitations, and yet sufficiently challenging to use up both semesters. The team had the personal goal of delivering a final product that would be exciting and that they would be proud to present to their peers and mentors.

The second phase of the project can be summarized as each team member searching for electronic components that would realize the desired functionality. This process consisted of identifying an aspect of the prototype's desired functionality, deciding on a design approach, and using that approach to find components that would fulfill the requirements. If parts could not be found, the design approach would be altered, and this process would repeat until a solution emerged. During this phase of design, project mentor Jon Gilreath proved invaluable due to his years of experience working with digital hardware. Many of the components which were ultimately selected were based on his recommendations, since they were often parts that were field–proven from use in numerous Honeywell Aerospace products.

The final major design effort was to create a PCB and additional circuitry to ensure that the design components would interface nicely with one another without any conflicts. Team member John Silvester led this portion of the design process due to his previous professional experience with PCB layout, but it was still a collaborative and educational effort with each other team member reviewing and verifying the schematics and footprint dimensions and deliberating on design decisions such as how to handle impedance matching of the high–speed signal traces.

Once the PCB order was placed, the prototype was assembled using a mixture of wire soldering and heat gun reflow techniques. The device was then delivered to the mentors at Honeywell for verification. After some initial hiccups and troubleshooting, the device operated and passed all tests used to prove functionality.

After much research and design effort, Team 23 was able to produce a working prototype of a fiber optic–copper bidirectional gigabit Ethernet media converter that met the design specifications set in the early stages of the first semester. The final design struck a balance of cost, manufacturability, uniqueness, and robustness. The final product seems strikingly simple by design, but represents a great deal of deliberation and careful decision making to leverage various products available on the market. Rather than trying to reinvent the wheel and design from the ground–up, the team split the design into a few functionality–blocks, then focused on making those portions integrate well with each other on a very cleanly laid–out PCB with minimal opportunity for failure.

If work is to be continued, Team 23's prototype acts as a design proposal that demonstrates the desired functionality is possible using these COTS components. This prototype could be redesigned by taking these larger circuit elements (such as the SFP module and DC/DC converter) and breaking them into smaller subcomponents in order to obtain finer control over device specifications and reduce manufacturing costs by eliminating unused functionality.

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Appendix A Figures

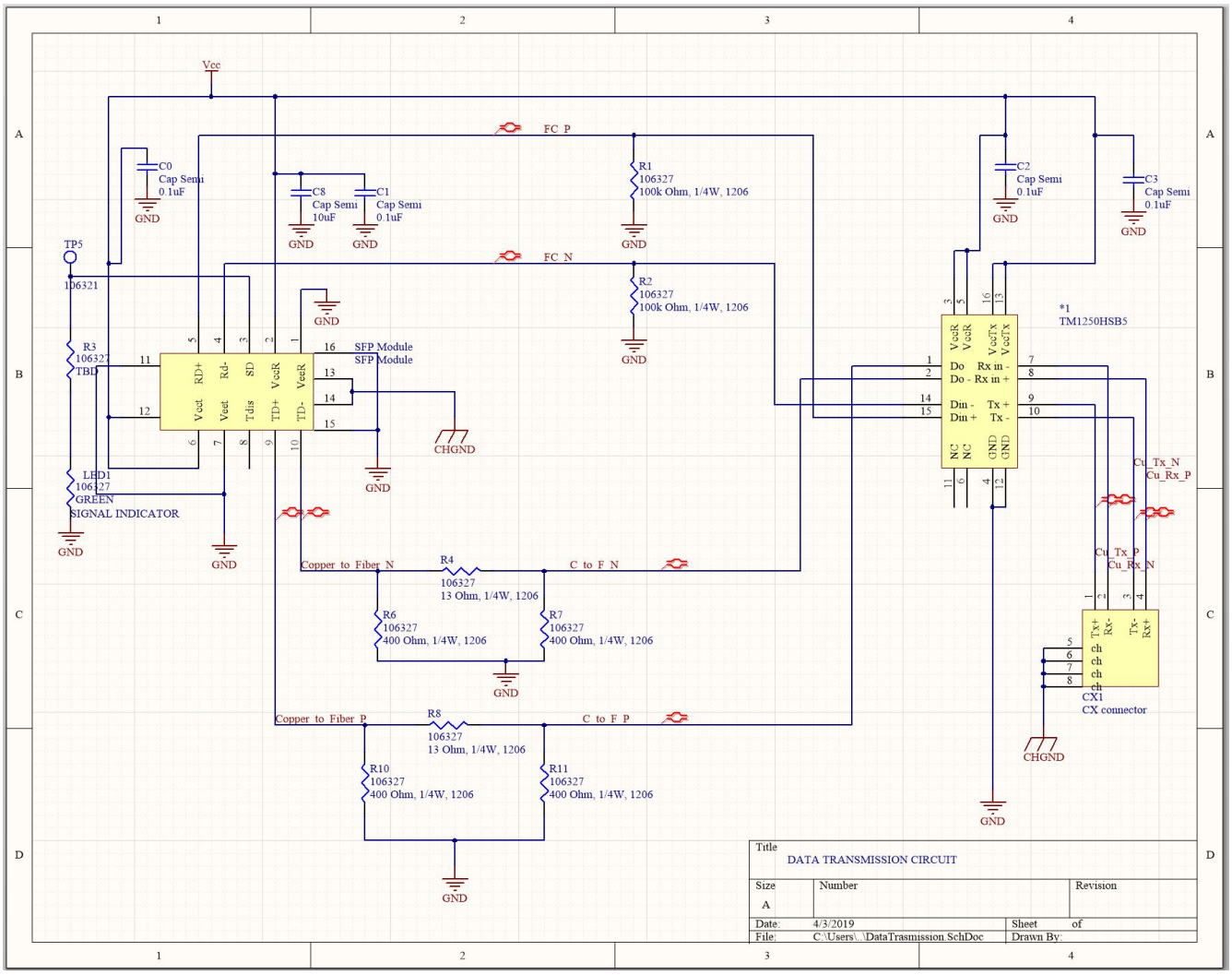


Figure 11: The full circuit schematic for the signal reception, conversion, and transmission paths used to create the PCB.

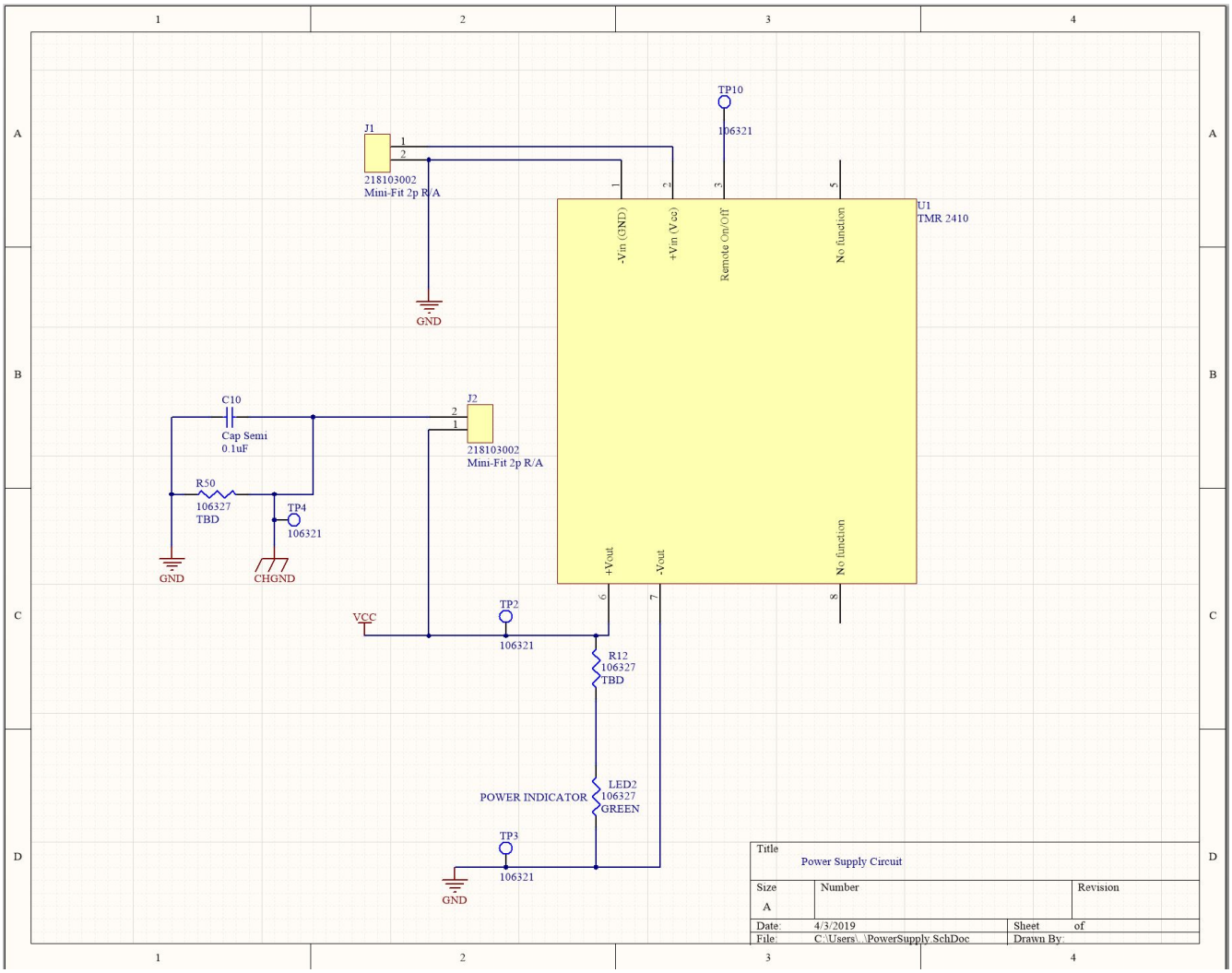
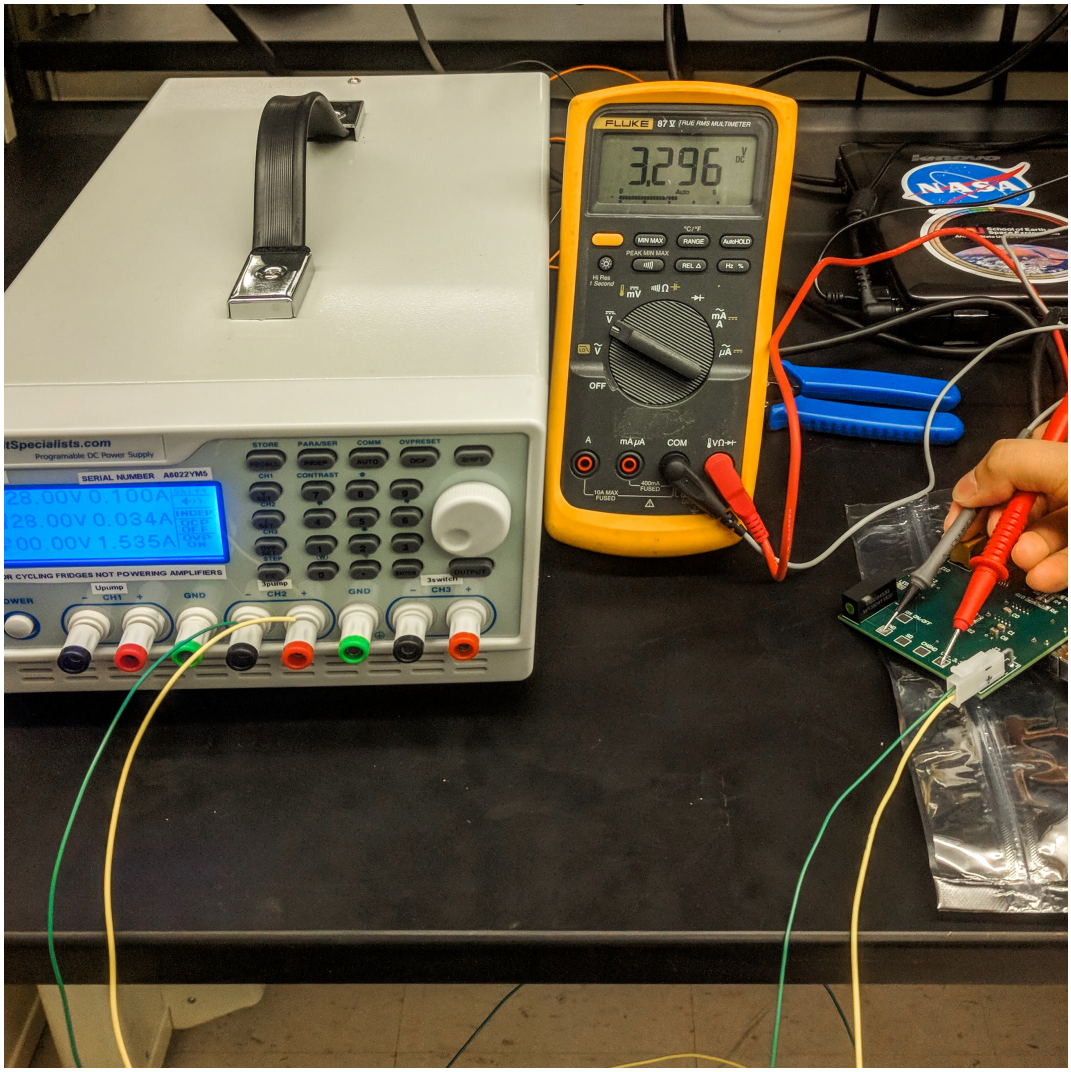
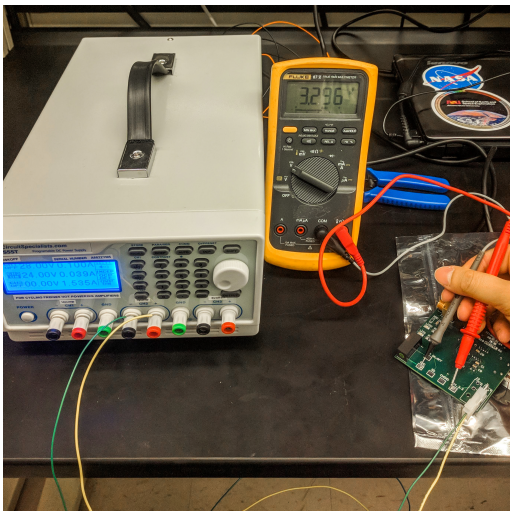


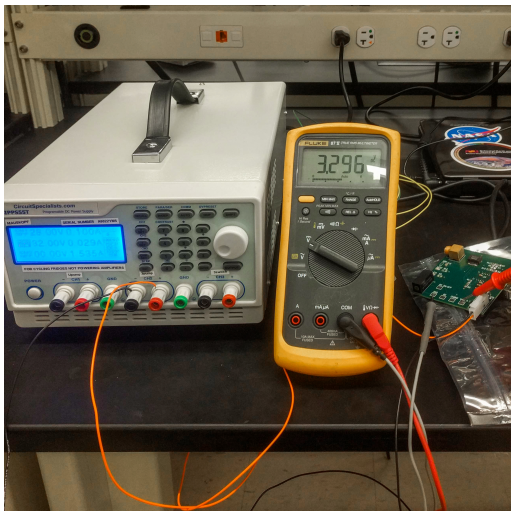
Figure 12: The circuit schematic for the power supply used to create the PCB.



(a) 28 V



(b) 24 V



(c) 32 V

Figure 13: The power conversion to varying input levels.

Appendix B Tables

Component	Reference Name(s)	Quantity	Unit Price
TRACO TMR 2410		1	\$16.05
PulseR TM1250HSB5		1	\$72.85
Avago HFBR5911LZ		1	\$52.50
Amphenol quadrax receptacle		1	\$262.71
Mini–Fit connector		2	\$0.57
PCB		1	\$66.00
100 kΩ 1206 SMD resistor	R_1, R_2	2	\$0.10
68 Ω 1206 SMD resistor	R_3	1	\$0.10
13 Ω 1206 SMD resistor	R_4, R_8	2	\$0.11
0 Ω 1206 SMD resistor	R_5	1	\$0.07
390 Ω 1206 SMD resistor	R_6, R_7, R_{10}, R_{11}	4	\$0.47
10 Ω 1206 SMD resistor	R_12	1	\$0.10
0.1 μF 1206 SMD capacitor	C_0, C_1, C_2, C_3, C_{10}	5	\$0.81
10 μF 1206 SMD capacitor	C_8	1	\$3.08
LED 1206 SMD (green)	LED_1, LED_2	2	\$0.34
Total Cost			\$481.66

Table 8: The total cost of the prototype.

Item	Quantity	Order Price	Notes
TRACO TMR 2410	3	$48.15	
Maxim MAX3711ETG+	3	$20.47	Not used due to size concerns
PulseR TM1250HSB5	3	$0.00	Obtained free samples from manufacturer
Avago HFBR5911LZ	2	$0.00	Provided by Honeywell
Amphenol quadrax receptacle	2	$0.00	Provided by Honeywell
Mini–Fit connector	2	$0.00	Already owned
PCB	2	$167.70	
100 kΩ 1206 SMD resistor	5		
68 Ω 1206 SMD resistor	3		
13 Ω 1206 SMD resistor	5		
0 Ω 1206 SMD resistor	10		
390 Ω 1206 SMD resistor	10	$44.89	
10 Ω 1206 SMD resistor	3		
0.1 μF 1206 SMD capacitor	10		
10 μF 1206 SMD capacitor	3		
LED 1206 SMD (green)	4		
YIHUA 8786D Soldering Station	1		
No–clean solder wick	1	$111.51	
Solder paste, 15 g	1		
Solder flux pen, 10 mL	1	$9.03	
Helping Hands magnifying glass	1	$31.58	
Lead–free solder wire, 0.6 mm, 50 g	1		
Total Cost		$433.33	

Table 9: The total cost of the project.